What is claimed is:

1. A data latch circuit, comprising:

a sense amplifying unit outputting a first signal in response to input data, a first inverted signal in response to a clock signal, a second signal in response to given cascode data, and a second inverted signal in response to the clock signal;

a clock latch unit generating a gated clock signal for enabling output of the cascode data to the sense amplifying unit, in response to an enabling signal and the clock signal; and

a multiplexer unit outputting the first signal as output data and the first inverted signal as feedback data, or outputs the second signal as output data and second inverted signal as feedback data, based on a logic level of the enabling signal.

2. The circuit of claim 1, wherein

the first signal is output as output data the first inverted signal is output as feedback data, if the enabling signal is at a first logic level, and

the second signal is output as output data and the second inverted signal is output as feedback data, if the enabling signal is at a second logic level.

3. The circuit of claim 1, further comprising a cascode logic unit storing the output data and feedback data and generating the cascode data in response to the gated clock signal.

4. The circuit of claim 1, wherein

the logic level of the first signal is the same as the logic level of the input data,

the logic level of the first inverted signal is opposite to the logic level of the first signal,

the logic level of the second signal is the same as the logic level of the cascode data, and

the logic level of the second inverted signal is opposite to the logic level of the second signal.

5. The circuit of claim 1, wherein the gated clock signal is enabled when both the enabling signal and the clock signal are synchronized at the same logic level.

6. The circuit of claim 3, wherein the sense amplifying unit includes:

a first sense amplifier receiving the input data and outputting the first signal in response to the input data, and receiving the clock signal and outputting the first inverted signal in response to the clock signal; and

a second sense amplifier receiving the cascode data from the cascode logic unit and outputting the second signal in response to the cascode data, and receiving the clock signal and outputting the second inverted signal in response to the clock signal.

7. The circuit of claim 1, wherein the multiplexer unit includes:

a first selection unit receiving the first signal via a first terminal and the second signal via a second terminal, outputting the first signal as output data when the enabling signal is at the first logic level and outputting the second signal as output data when the enabling signal is at the second logic level; and

a second selection unit receiving the first inverted signal via a first terminal and the second inverted signal via a second terminal, outputting the first inverted signal as feedback data when the enabling signal is at the first logic level and outputting the second inverted signal as feedback data when the enabling signal is at the second logic level.

8. The circuit of claim 1, wherein the first selection unit and the second selection unit are multiplexers.

9. The circuit of claim 1, wherein the clock latch unit includes:

an inverter generating an inverted signal of the clock signal;

a latch receiving the enabling signal and activated in response to the inverted clock signal; and

a logical multiplier calculating a logic multiplication of an output of the latch and the clock signal for generating the gated clock signal.

10. The circuit of claim 1, wherein the enabling signal is activated prior to activation of the clock signal.

11. A data latch circuit, comprising:

a first data transmission unit receiving input data and generating output data in response to an enabling signal;

a second data transmission unit receiving given cascade data and generating feedback data in response to the enabling signal;

the first data transmission unit further receiving a given second signal from the second data transmission unit in response to a clock signal,

the second transmission data unit further receiving a first inverted signal from the first data transmission unit in response to the clock signal,

a clock latch unit generating a gated clock signal in response to the enabling signal and the clock signal; and

a cascode logic unit storing the output data and the feedback data and generating the cascode data in response to the gated clock signal.

12. The circuit of claim 11, wherein the gated clock signal is enabled when the enabling signal and the clock signal are synchronized at the same logic level.

13. The circuit of claim 11, wherein the first data transmission unit includes:

a first sense amplifier outputting a first signal in response to the input data and the first inverted signal in response to the clock signal, wherein the logic level of the first signal is the same as the logic level of the input data, and wherein the logic level of the first inverted signal is opposite to the logic level of the first signal; and

a first selection unit receiving the first signal via a first terminal and the second signal via a second terminal, outputting the first signal as the output

data when the enabling signal is at a first level, and outputting the second signal as the output data when the enabling signal is at a second level.

14. The circuit of claim 13, wherein the first selection unit is a multiplexer.

15. The circuit of claim 11, wherein the second data transmission unit includes:

a second sense amplifier receiving the cascode data from the cascade logic unit and outputting the second signal, wherein the logic level of the second signal is the same as the logic level of the cascode data, and outputting the second inverted signal in response to the clock signal, wherein the logic level of the second inverted signal is opposite to the logic level of the second signal; and

a second selection unit receiving the first inverted signal via a first terminal and the second inverted signal via a second terminal, outputting the first inverted signal as the feedback data when the enabling signal is at a first level, and outputting the second inverted signal as the feedback data when the enabling signal is at a second level.

16. The circuit of claim 15, wherein the second selection unit is a multiplexer.

17. The circuit of claim 11, wherein the clock latch unit includes:

an inverter generating an inverted signal of the clock signal;

a latch receiving the enabling signal and activated in response to the inverted clock signal; and

a logical multiplier calculating a logic multiplication of an output of the latch and the clock signal for generating the gated clock signal.

18. The circuit of claim 11, wherein the enabling signal is activated prior to activation of the clock signal.

19. A data transmission unit, comprising:

a sense amplifier outputting a first signal in response to input data, the logic level of the first signal is the same as the logic level of the input data; and

a multiplexer receiving the first signal via a first terminal and receiving a second signal generated externally from the data transmission unit via a second terminal, outputting one of the first signal and second signal as output data based on a logic level of an enabling signal applied thereto.

20. The unit of claim 19, wherein the multiplexer outputs the first signal as output data if the enabling signal is at a first logic level, and outputs the external second signal as the output data if the enabling signal is at a second logic level.

21. A method of improving operating speed in a circuit, comprising:

generating a first signal in response to input data and a first inverted signal in response to a clock signal;

generating a second signal in response to given cascode data and a second inverted signal in response to the clock signal;

outputting one of the first signal and second signal as output data and one of the first inverted signal and second inverted signal as feedback data based on a logic level of an enabling signal.

22. The method of claim 21, wherein the outputting step includes

outputting the first signal as output data and the first inverted signal as feedback data, if the enabling signal is at a first logic level, and

outputting the second signal as output data and the second inverted signal as feedback data, if the enabling signal is at a second logic level.

23. The method of claim 21, further comprising:

storing the output data and feedback data.

24. The method of claim 21, further comprising:

generating a gated clock signal in response to an enabling signal and the clock signal; and

generating the cascode data in response to the gated clock signal, the cascade data including the output data and feedback data.

25. The method of claim 24, further comprising activating the gated clock signal when both the enabling signal and the clock signal are synchronized at the same logic level.

26. The method of claim 21, wherein

the logic level of the first signal is the same as the logic level of the input data,

the logic level of the first inverted signal is opposite to the logic level of the first signal,

the logic level of the second signal is the same as the logic level of the cascode data, and

the logic level of the second inverted signal is opposite to the logic level of the second signal.

27. A data latch circuit configured with improved operating speed in accordance with the method of claim 21.

28. A data latch circuit employing the data transmission unit of claim 19.

29. A data transmission unit for a data latch circuit configured with improved operating speed in accordance with the method of claim 21.